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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/751,523	01/06/2004	Takaki Yoshida	60188-745	3277

7590 09/26/2006

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EXAMINER

KIK, PHALLAKA

ART UNIT PAPER NUMBER

2825

DATE MAILED: 09/26/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/751,523

Applicant(s)

YOSHIDA, TAKAKI

Examiner

Phallaka Kik

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 06 January 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-11 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 10 and 11 is/are rejected.
- 7) ☒ Claim(s) 1-9 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 06 January 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|----------------------------------------------------------------------------------------|-------------------------------------------------------------------|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date <u>1/6/2004</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. This Office Actions responds to the Application and IDS filed on 1/6/2004.

Claims 1-11 are pending.

Priority

2. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Claim Objections

3. **Claims 1-11** are objected to because of the following informalities:

As per **claim 1**, "the number" (line 6) should be --a number-- for proper antecedent basis.

As per **claim 2**, "the step" (line 2) should be --a step-- and "the variation" (line 3) should be --a variation-- for proper antecedent basis.

As per **claim 5**, "the operation" (line 2) should be --an operation-- for proper antecedent basis.

As per **claim 6**, "the step" (line 2) should be --a step-- and "the operation" (line 3) should be --an operation-- for proper antecedent basis.

As per **claim 7**, "the step" (line 2) should be --a step-- for proper antecedent basis.

As per **claims 2-7**, the claims are also objected to for incorporating the above errors into the respective claims by claim dependency.

As per **claim 8**, "the number" (line 2) should be --a number-- for proper antecedent basis.

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As per **claim 9**, "the number" (line 6) should be --a number--; "the configuration" (lines 8 and 9) should be --a configuration-- for proper antecedent basis.

As per **claim 10**, "the number" (line 7) should be --a number-- for proper antecedent basis.

As per **claim 11**, "the number" (line 7) should be --a number--; "the configuration" (lines 9 and 10) should be --a configuration-- for proper antecedent basis.

Appropriate correction is required.

Claim Rejections - 35 USC § 101

4. 35 U.S.C. 101 reads as follows:

Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

5. **Claims 10-11** is rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter, wherein "the detecting program" and "the layout program" are directed to computer program per se which are not embodied in a computer-readable medium is non-statutory because they are not capable of causing functional change in the computer (see Warmerdam, 33 F. 3d at 1361, 31 USPQ2d at 1760).

Allowable Subject Matter

6. **Claims 1-11** would be allowable if rewritten or amended to overcome the objections due to the noted informalities and the rejection(s) under 35 U.S.C. 101, set forth in this Office action.

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7. The following is a statement of reasons for the indication of allowable subject matter:

As per **claims 1-7,10**, the independent claims 1 and 10, from which the respective claims depend, recite the error portion detecting method/program for a semiconductor integrated circuit, comprising the inventive steps/means of estimating a supply voltage variation level based on the number of circuit elements which is detected at the simultaneous-operation circuit element number detecting step based on the transition timing detecting step as claimed. In particular, the prior arts made of record teach various methods/systems of detecting transition timing and circuit layout having the particular transition timing (see especially **Khouja et al.**, U.S. Patent No. 6,345,379, especially Fig. 2 and col. 11, lines 23-63; **Hathaway et al.**, U.S. Patent Application Publication No. 2003/0226122, especially paragraphs [0011]; **Lin et al.**, U.S. Patent Application Publication No. 2003/0212538, especially paragraphs [0044]-[0047]; **Thill**, U.S. Patent No. 6,370,674, especially col. 7, line 66 to col. 8, line 25; **Hathaway et al.**, U.S. Patent No. 6,615,395, especially col. 6, line 4 to col. 7, line 55; **Sander et al.**, U.S. Patent No. 5,047,967, especially col. 7, lines 10-18; **McElvain et al.**, U.S. Patent Application Publication No. 2006/0095872, especially paragraphs [0078], [0082], [0100], [0145]). However, none of the prior arts made of record, alone or in combination, teach the inventive steps/means as claimed. Accordingly, the claimed invention is novel and un-obvious over the prior arts made of record.

As per **claim 8**, the claim recites an error portion detecting method for a semiconductor integrated circuit comprising the inventive steps of estimating the supply

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voltage variation level based on the number of detected at the circuit number detection step as claimed, which the prior arts made of record failed to teach or suggest. In particular, the prior arts made of record teach various methods/systems for detecting transition timing and circuit layout having the particular transition timing (see especially prior arts recited above). However, none of the prior arts made of record, alone or in combination, teach the inventive steps/means as claimed. Accordingly, the claimed invention is novel and un-obvious over the prior arts made of record.

As per **claims 9,11**, the claims recite the layout method/program for a semiconductor integrated circuit comprising the inventive steps/means of determining the configuration of the circuit elements or the configuration of the power supply lines based on the number of circuit elements which is detected at the simultaneous-operation circuit element number detecting, such that any of the circuit elements is supplied with the supply voltage through a power supply line different from the common power supply line, as claimed, which the prior arts made of record failed to teach or suggest. In particular, the prior arts made of record teach various methods/systems for detecting transition timing and circuit layout having the particular transition timing (see especially prior arts recited above). However, none of the prior arts made of record, alone or in combination, teach the inventive steps/means as claimed. Accordingly, the claimed invention is novel and un-obvious over the prior arts made of record.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Therefore, Applicant is requested herein to consider them carefully in response to this Office Action.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phallaka Kik whose telephone number is 571-272-1895. The examiner can normally be reached on Monday-Thursday, 8:30AM-7PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571-272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Any response to this action should be mailed to:

Commissioner for Patents

P. O. Box 1450

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Alexandria, VA 22313-1450

or faxed to:

571-273-8300

A handwritten signature in black ink, appearing to read "Phallaka Kik", written in a cursive style.

Phallaka Kik

Primary Examiner

September 16, 2006